Self Cascode Current Mirrors For Low Voltage Analog Circuits

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Abstract: A current mirror (CM) based on self cascode arrangement, useful for low voltage analog and mixed mode circuit is proposed. The CM uses 4 MOSFETs, has high input and output swing, operating at ± 0.5 V supply. Pspice simulations confirm the high performance of this CM having a bandwidth of 2.1 GHz. Resistive and capacitive compensations result in about threefold bandwidth increase to 6.1 GHz.

Key words: Current mirrors, regulated cascode, self cascode structure

INTRODUCTION

The market and the need to develop efficient portable electronic equipments have pushed the industry to produce circuit designs with very low voltage (LV) power supply and often constrained to low power consumption. This trend towards minimized circuits has given a strong and decisive boost towards the design of low voltage low power (LVLP) analog integrated circuit design.

In all analog and mixed mode VLSI circuits, a CM is an essential requisite for all signal processing elements. In this paper, we have investigated the merits and demerits of self cascode approach: a promising low voltage analog design technique. Two CM structures have been explored and implemented. Their properties have been compared with the conventional and regulated structures. Analysis of these CMs have been done using P-Spice simulations for 0.13 micron CMOS technology.

1. The Current Mirror

In a conventional CM structure Figure 1, $V_{in}$ depends on the biasing conditions of M1 which operates in saturation mode [ALL 87]. For this CM,

$$I_{in(sat)} = \frac{\beta}{2} (V_{GS} - V_T)^2$$  (1)

The output compliance voltage required for this CM is given by [ALL 87] [RAJ 00].

$$V_{out} = V_{DS(sat)} = V_T + \frac{2I_m}{\beta}$$  (2)

Figure 1. Conventional level shifter CM structure

Hence it suffers from the drawback that it requires an input compliance voltage which is greater than one threshold ($V_T$). Moreover the output impedance of this structure is very low [ALL 87], ($r_{out} = 1/g_m = 1/\beta I_D$) and the effect of channel length modulation too causes significant error in copying currents, especially if minimum length transistors are used. Hence, this structure cannot be used in LV applications.
2. Cascode Structures

The cascode connection is an effective method to suppress the channel-length modulation and thus enhance the working. Here the cascode device “shields” the bottom transistor from variations in the output, which results in high output impedance. It also reduces the ratio errors due to difference in output and input voltages [SAC 90] [MIL 87] [ALL 87].

The idea behind cascode structure is to convert the input voltage to a current and apply the result to a common source stage. This has been employed in various LV topologies [ALF 95] [GIV 03] [RAJ 02a] [LI 03]. This is employed in regulated cascode Figure 2 to increase the output resistance to $g_m^2 r_{ds}^3$ [ALL 87] [RAJ 00].

The cascode structure is also used for a PMOS–NMOS combination which performs the same function. Figure 3 is called “folded cascode”, used to alleviate the drawback of telescopic cascode’s, limited output swings and difficulty in shorting the input and output [MIL 87] [ALL 87]. Primary advantage of folded structure lies in the choice of the voltage levels, because it does not “stack” the cascode transistor on top of the input device. However, this structure generally consumes higher power.

3. Self Cascode Technique for LV Topologies

As the device sizes are shrinking fast, the output impedance of the MOSFET is also reducing due to the channel length modulation and these short channel MOSFETs cannot provide high gain structures. To have high output impedance and thereby high gains, cascoding is done. The regular cascode structures are avoided as their use increases the gain of the structure, but decreases the output signal swing. Self-cascode (SC) is the new technique, which does not require high compliance voltages at output nodes. The two distinct advantages are, firstly, it provides higher output impedance and secondly, it reduces the effect of miller capacitance on the input of the amplifier [MUL 96].

A SC is a 2-transistor structure [COM 03] [COM 04] [RAJ 02a] Figure 4a, which can be treated as a single composite transistor Figure 4b. The composite structure has both the gates of M1 & M2 driven by the input signal and share a single bias source $V_{GG}$. If M2 and M1 have similar W/L aspect ratio, M1 will operate in the triode region while M2 will operate in the active region. In this case, the composite cascode works like a common-source stage, but with higher voltage gain. If M2 is chosen with a much higher aspect ratio than M1, then with appropriate bias of $V_{GG}$ and $I_{bias}$, M1 is placed in the strong inversion region while M2 operates in the weak inversion region [COM 03] [COM 04]. The gain in this case is further increased.

![Figure 2: Regulated Cascode level shifter CM structure](image)

![Figure 3: Folded Cascode](image)

![Figure 4: (a) Self Cascode NMOS Structure (b) Equivalent NMOS transistor](image)

Thus, in a SC structure M1 operates in linear region, while M2 operates in saturation or linear region [ZEK 97] [COM 03]. Hence, voltage between source and drain of M1 is small. There is no appreciable difference between the $V_{Dsat}$ of composite and simple transistors and a self-cascode can be used in low voltage operation [COM 03] [COM 04].

The advantage offered by SC structure is that it offers high output impedance similar to a regular cascode structure while output voltage requirements are similar to that of a single transistor [RAJ 02b]. Its drawbacks are limited input common mode range, small output swing and relatively high power supply requirements [COM 04] [SAN 99].

4. Self Cascode CM Structures

SCCM-1: This proposed LVCM is shown in Figure 5. M1 & M2, M3 & M4, M7 & M8 are pairs of
composite cascode structures. They have replaced M1, M2 & M3 (Figure 9) [RAJ 02c]

SCCM-2: This proposed LVCM is shown in Figure 6.

The most optimum aspect ratios chosen for different transistors are given in Table 1. Both the circuits are simulated for 0.13 µm technology with level 7 parameters to give optimum results as discussed in Section VI. Ibias3 and Ibias4 (SCCM-1) are assumed to be 5µA and 100µA respectively. The selection criterion for Ibias3 is to ensure lower \( V_{in} \) and Ibias4 is selected to ensure ON condition for M6. Ibias1 (SCCM-2) is assumed to be 5 µA. All the circuit operations are simulated for supply voltage of ±0.5 V.

![Figure 5: Self Cascode Current Mirror–1 (SCCM-1)](image)

![Figure 6: Self Cascode Current Mirror-2 (SCCM-2)](image)

5. Performance Evaluation

The comparison between the various small signal parameters of SCCM-1, SCCM-2, regulated and conventional CM (level shifter structure) are tabulated in Table 2. It is clearly seen that SCCM-2 has better trade off in the area (4 MOSFETS with one bias current) and for input and output compliance voltages. It has a reasonably good bandwidth, low input resistance and comparatively high output resistance. The current transfer characteristic of SCCM-2 is shown in Figure 7 and the input characteristics in Figure 8. For \( I_{in} \) of 100 µA the 3db bandwidth comes out to be 2.1 GHz. The bandwidth for \( I_{in} \) of 150µA is 2.3 GHz, and that for 200 µA is 2.5 GHz. Thus bandwidth is shown to be a function of \( I_{in} \).

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>SCCM-1</th>
<th>SCCM-2</th>
<th>Regulated cascode</th>
<th>Conv. CM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer Ratio ( I_{out}/I_{in} )</td>
<td>0.91</td>
<td>.94</td>
<td>0.88</td>
<td>0.98</td>
</tr>
<tr>
<td>I/P resistance ( (KΩ) )</td>
<td>1.3</td>
<td>1</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>O/P resistance</td>
<td>89 KΩ</td>
<td>0.62 MΩ</td>
<td>2.9 MΩ</td>
<td>18 KΩ</td>
</tr>
<tr>
<td>Power dissipation ( (mW) )</td>
<td>0.2</td>
<td>0.2</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>I/P compliance voltage ( (mV) )</td>
<td>300</td>
<td>290</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>O/P compliance voltage ( (mV) ) (across MOSFETs)</td>
<td>380 (4)</td>
<td>300 (2)</td>
<td>340 (2)</td>
<td>210 (one)</td>
</tr>
<tr>
<td>Bandwidth ( (GHz) )</td>
<td>1.4</td>
<td>2.1</td>
<td>8.8</td>
<td>14</td>
</tr>
<tr>
<td>Area ( ) (no. of MOSFETs)</td>
<td>8</td>
<td>4</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>Bias currents ( (µA) )</td>
<td>Ibias1= 5</td>
<td>Ibias2= 100</td>
<td>Ibias1= 5</td>
<td>Ibias2= 20</td>
</tr>
</tbody>
</table>

The influence of gate resistances at M1, M2, M3 of SCCM-2 over the bandwidth are shown in Figure 9. The gate resistance at M1 (3 KΩ) increases the bandwidth to 2.2 GHz and for 5KΩ to 2.3 GHz. The capacitance in between the drain and gate of M1
increases the bandwidth to 4.2 GHz. The bandwidth improves by threefold when both resistance and capacitor are included, it comes out to be 6.1 GHz (for \( R_g = 3 \text{ K} \) and \( C = 10 \text{ nF} \)). The effect of resistive and capacitive compensation at M1 of SCCM-2 is shown in Figure 10. The effect of gate resistances at M2 and M3, on the bandwidth of SCCM-2 structure is given in Table 3. It is seen that there is degradation of bandwidth when they are included.

<table>
<thead>
<tr>
<th>Gate Resistances</th>
<th>Resistive value in KΩ</th>
<th>Bandwidth in GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>At the Gate of M2 in KΩ</td>
<td>1</td>
<td>2.12</td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td>2.12</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>2.08</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>2.04</td>
</tr>
<tr>
<td>At the Gate of M3 in KΩ</td>
<td>1</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1.24</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>Both R2 and R3</td>
<td>1.5</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Figure 7. Current Transfer Characteristics of SCCM-2

Figure 8. Comparison Input Characteristics between SCCM-1 and SCCM-2

The comparison of the output current to applied drain bias characteristics for CMs is shown in Figure 11. The output characteristics at low input currents for SCCM-2 are shown in Figure 12. An offset current of 360 nA occurs at \( I_{in} = 0 \text{A} \). Figure 13 shows the characteristics at high currents.
6. Conclusion

This article has shown the self cascode approach, for the key signal processing block i.e. CM. Two such structures have been presented. The SCCM-2 (4 MOSFETs) with input resistance of 1 KΩ, output resistance of 0.62 MΩ and bandwidth of 2.1 GHz is a promising option for sourcing a mirrored current into high impedance output node of other signal processing circuits. Its comparison with other SC structure, regulated and conventional structures indicate that self cascode approach is a good solution for low voltage applications.

REFERENCES


