A Comparison Study of Electrical Characteristics of Schottky Source Drain and Doped Source Drain Double Gate SOI MOSFET

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Abstract: A simulation study has been carried out on a Schottky (metal) source drain (S/D) double gate (DG) SOI MOSFET. Unlike the doped S/D structure, this device can operate both in accumulation and inversion mode. Tunneling is the dominant current mechanism in Schottky S/D DG SOI MOSFET. A comparison study has been performed between metal S/D double gate SOI MOSFET and a similar structure with doped S/D. For the gate length $L_G = 20\text{nm}$, metal source/drain structure has better $(I_{on}/I_{off})$ ratio than that of doped S/D structure. Reducing Schottky barrier height (SBH) improves $(I_{on}/I_{off})$ and transconductance ($g_m$) in Schottky S/D DG SOI MOSFET. Gate Induced Drain Leakage current is much smaller in doped S/D structure than in Schottky S/D DG SOI MOSFET. Increasing S/D underlap reduces $I_{off}$ in both structures. A reduction in gate voltage results in a reduction of depletion layer width at source side and thus results in a reduction of $g_{m}$. 

Key words: Metal Source Drain MOSFET, Double Gate SOI MOSFET, Electrical characteristics, Gate Induced Drain Leakage.

INTRODUCTION

Ultra thin body double gate SOI MOSFET is considered one of the most promising candidates for sub-30nm MOSFET scaling. This structure has good short channel behavior, low leakage current, small subthreshold swing and better scalability than the conventional bulk MOSFET. Using ultra shallow body leads to suppression of short channel effects (SCE) in CMOS technology. However the design of ultra shallow junction is susceptible to a high series resistance problem which degrades device’s performance [1]. To overcome this scaling difficulty, Schottky Source/Drain MOSFETs have been proposed as a substitute for doped S/D structure in the nanometer regime [2]. Schottky Barrier Double Gate SOI MOSFET (SB-DG MOS) offers several advantages such as low parasitic S/D resistance, abrupt junctions at source/drain body interface that enables physical scaling of the device to sub 30-nm gate length, low temperature processing for the formation of S/D, two fewer mask in the formation of Schottky CMOS in comparison with doped structure and superior control of the off-state leakage current due to intrinsic Schottky barrier. There is no need for extra doping in the channel. Thus scattering may be decreased and mobility may be enhanced.

In this paper, we have performed a simulation study on a double gate MOSFET with metal source drain. We will first give a brief discussion of its principles of operation. Tunneling is identified as the dominant current component in this device. In section 2 we will investigate the effect of the tunneling current on the $(I_{on}/I_{off})$ ratio and in section 3 we will compare SB-DG MOS electrical characteristics including transconductance, $(I_{on}/I_{off})$ ratio, Gate induced drain leakage current(GIDL) and the effect of S/D underlap $(L_{un})$ with a similar structure having doped source drain.

Simulations were carried out using dessis7, from ISE TCAD. Following models in our simulation study were included: Hydrodynamic model for carrier transport, Vandort model for Quantum Correction, Shockley Read Hall (SRH) for Recombination and Philips model for the mobility. This model accounts for the temperature dependence of the mobility, electron–hole scattering, screening of ionized impurities by charge carriers, clustering of impurities and the effect of
vertical electric field on the carrier mobility.

Figure 1.a shows double gate SOI MOSFET with metal source/drain. Double Gate SOI MOSFET with doped source drain is presented in Figure 1.b. The structural parameters of the devices that have been studied in this paper are presented in table 1.

![Figure 1: (a) Schottky S/D DG-SOI-MOSFET, (b) Doped S/D DG-SOI-MOSFET.](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Length</td>
<td>20nm</td>
</tr>
<tr>
<td>Body thickness</td>
<td>10nm</td>
</tr>
<tr>
<td>Channel doping</td>
<td>1E15(Arsenic),(Boron)</td>
</tr>
<tr>
<td>Doped S/D doping</td>
<td>2E20(Arsenic)</td>
</tr>
<tr>
<td>Metal resistivity</td>
<td>0.027 Ω·µm</td>
</tr>
<tr>
<td>Gate dielectric stack</td>
<td>0.5nm of SiO₂ under 2.5nm of high k, EOT=1nm</td>
</tr>
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**Table 1: Device’s Parameters.**

1. **Principles of operation**

Figure (2) illustrates conduction band diagram for the n-body SB-DG MOS for nonnegative gate voltages. In equilibrium condition i.e. \( V_G = 0V, V_D = 0V \), the barrier width at S/D side is not thin enough for carriers to tunnel through and only thermionic emission occurs, in which carriers with energy above the barrier height can pass over the Schottky barrier. The case \( V_G = 0V, V_D = 0.05V \) represents the conduction band for the off condition in this device. As \( V_G \) is increased, \( V_G = 0.8V, V_D = 0.05V \), band bending in the semiconductor at the metal/semiconductor interface increases and eventually reaches to the point at which carriers find a high probability of tunneling through the sufficiently narrowed barrier[3]. By applying a negative gate bias to this n-body SB-DG MOS, the body region depletes and finally inverts to form a p-type channel as shown in Figure(3).

![Figure 2: Conduction band diagram for n-body Schottky S/D DG-SOI-MOSFET for positive gate and drain voltages.](image)

It can be concluded that SB-DG MOS can operate both in accumulation and inversion mode. So unlike doped S/D structure, SB-DG-MOS is ambipolar device i.e. electrical characteristics of both NMOS and PMOS are attainable on a single body [4].

2. **The effect of tunneling on the \( \frac{I_{on}}{I_{off}} \) ratio**

It is well known that SB-DG-MOS has two current components: the thermionic emission and the tunneling component. WKB approximation has been used for simulating tunneling current. In order to determine the dominant current component, two sets of simulations have been carried out (one, including barrier tunneling and the other, without barrier tunneling). \( \frac{I_{on}}{I_{off}} \) was extracted from these data. According to ITRS\(^1\), \( I_{off}=1nA \) is expected for devices with \( L_G=20nm \). We have tuned gate work function to meet \( I_{off}=1nA \). Figure (4) illustrates the result of two

\(^1\) International Technology Road Map for Semiconductors.
sets of simulation for different Schottky barrier heights (SBHs). It is seen that \( \frac{I_{on}}{I_{off}} \) is larger than the case where barrier tunneling is absent. It can be concluded that tunneling is the dominant current mechanism and is controlled by the gate voltage. Gate voltage modulates the barrier width at S/D body interface by accumulating or depleting majority carriers at the interface.

**3. Comparison with doped structure**

**3.1. \( \frac{I_{on}}{I_{off}} \) Ratio**

For the sake of comparison, a simulation study has been carried out on a p-body SB-DG MOS with a similar doped structure. For \( L_G = 20 \text{nm} \), doped structure has larger \( I_{off} \) than that of SB-DG MOSFET. \( \frac{I_{on}}{I_{off}} \) for doped structure is approximately 3000. \( \frac{I_{on}}{I_{off}} \) ratio has been plotted for different SBHs in Figure 5 and the results have been compared with that of doped S/D structure. \( \frac{I_{on}}{I_{off}} \) ratio is larger for SB-DG MOS than that of doped S/D structure. It is concluded that in this scale, SB-DG MOS with a lower barrier height will be a good alternative for doped structure.

**3.2. Transconductance (gm)**

Increasing SBH leads to a reduction in the on-state current and thus in gm. gm for different SBHs and for doped structure has been plotted in figure (6).

![Figure 6: \( g_m \) for SB-DG MOS and doped S/D structure.](image)

We conclude from this figure that for SBHs larger than 150meV, doped structure has better gm than SB-DG MOS. SB-DG MOS has larger threshold voltage than doped S/D structure, thereby even for low SBHs, doped S/D structure has larger gm in subthreshold regime in comparison with SB-DG MOS. The lowest SBH that has been implemented corresponds to Erbium silicide (0.25eV) [4]. However, this structure has lower on-state current and gm than doped S/D structure.

**3.3. S/D Underlap Effect**

We have studied S/D underlap effect in SB-DG MOSFET and in doped S/D MOS structure for \( L_{un} = 0 \) nm up to \( L_{un} = 10 \) nm. Increasing \( L_{un} \) results in a reduction of \( I_{off} \) and \( I_{on} \) in both structures. Reduction of \( I_{off} \) can be related to reduction of drain voltage effect which results in Drain Induce Barrier Lowering (DIBL) in conventional doped S/D structure and Drain Induced Source Tunneling (DIST) in SB-DG MOS. DIST occurs in low \( V_G \) and high drain voltage in which large lateral electric field from drain can decrease the barrier width at source side and causes extra carrier tunneling from source in subthreshold regime [5]. On the other hand, on–state current reduces in both structures. In the doped S/D structure, increasing \( I_{on} \) results in an increase of barrier height and thus enhancement of threshold voltage, but in SB-DG MOS transistor, \( I_{on} \) reduces because of increase in barrier width at the source side which results in reduction of barrier tunneling current. Our simulation studies show that for \( L_{un} = 0 \) nm the barrier width is approximately 9nm and increases to 16nm for \( L_{un} = 10 \) nm.

Figure (7.a) shows transconductance in SB-DG-MOSFET structure versus underlap length and Figure (7.b) shows off-state current in SB-DG-MOSFET as a function of underlap length. Figure (8) shows off-state current in doped S/D structure versus underlap length.
Increasing underlap length leads to reduction of off-state current in both structures. SB-DG SOI MOSFET has smaller off-state current in comparison with doped S/D structure.

Figure 7: (a) $g_m$ for SB-DG MOS, (b) $I_{off}$ for SB-DG MOS versus $L_{un}$

Figure 8: $I_{off}$ versus $L_{un}$ for doped S/D structure.

4. Gate Induced Drain Leakage (GIDL) current

GIDL current results in an increase in $I_{off}$ in both structures. As was mentioned earlier, SB-DG MOS is an ambipolar device. One of the drawbacks of SB-DG MOS is that this device can not be completely switched off, because in low $V_G$ and high $V_D$, device tries to turn on in another direction and opposite type of carrier tunneling from drain occurs which enhances off-state leakage current. In our p-body NMOS, when $V_{GD}$ is negative, holes accumulate at drain/channel interface. In this case the barrier width for holes decreases and hole tunneling from drain side (GIDL) occurs. Hence aside from electron thermionic emission from source, GIDL contributes in off-state current enhancement. By reducing SBH for electrons, SBH for holes increases and leads to reduction of GIDL current Figure 9 compares GIDL current in SB-DG MOSFET and doped S/D structure. As it is shown in Figure (9), in this range of voltage, GIDL does not occur in doped structure. This is because conventional doped S/D structure is not ambipolar.

Figure 9: GIDL current for doped and Schottky S/D structure.

5. Conclusion

We have performed a simulation study on a nanoscale double gate SOI MOSFET with metal S/D rather than doped S/D structure. Simulations show that tunneling is the dominant current mechanism in SB-DG MOS. Comparing electrical characteristics of the SB-DG MOS to that of doped S/D structure reveals that ($I_{on}/I_{off}$) in SB-DG MOS is larger than the doped S/D structure. Reducing SBH results in better ($I_{on}/I_{off}$) in SB-DG MOS. Reducing SBH also improves $g_m$ in SB-DG MOS. Increasing S/D $L_{un}$ leads to a reduction of $L_{on}$ in both structures. $g_m$ reduces with increasing $L_{un}$ in SB-DG MOS. This is correlated with reduction in tunneling current. By reducing SBH, SB-DG MOS performance improves.

REFERENCES


