The Impact of Structural Parameters on the Electrical Characteristics of Nano Scale DG-SOI MOSFETs in Subthreshold Region

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Abstract: We explore the impact of structural parameters of nano scale Double Gate Silicon-On-Insulator MOSFETs (DG-SOI MOSFETs) on its electrical characteristics in subthreshold regime. In particular we show that increase in Source/Drain length (L_s/L_d) negligibly affects characteristics in this device for \(L_s/L_d \geq 30 \text{nm} \). However the fringing fields and effective gate capacitance \(C_{gd} \) increase with increasing \(L_s \) and \(L_d \). As the thin body thickness is decreased \(C_{gd} \) is increased and barrier height is decreased. However electron mobility also reduces and results in a decrease in drain current \(I_d \). This investigation also shows that an increase in gate overlap reduces both \(C_{gd} \) and DIBL effect, while \(L_g/L_d \) ratio is increased. These parameters affect the power consumption and device delay and can be useful in ultra thin body DGMOS design for low power applications.

Key words: Nano scale DG-SOI MOSFET – Source/Drain Length – Thin body -Gate overlap –Subthreshold regime – Effective gate capacitance -DIBL – Simulation.

INTRODUCTION

In recent years, power sensitive designs have attracted a lot of interests. This significant growth in demand is partly due to the need for battery-operated portable applications, such as, laptop computers, medical electronics, cellular phones, and other portable computing devices [1]. Digital circuits which work in subthreshold regime, use a supply voltage \(V_{dd} \) lower than threshold voltage \(V_{th} \), have smaller capacitance and require lower supply voltage than those which operate in the strong inversion regime. This makes them suitable for medium frequency, low power applications [2]. Numerous efforts have been performed for optimization of the devices for subthreshold operation. Due to their small junction capacitance and near ideal subthreshold slope DGMOS transistors are suitable for low power applications [3]. Furthermore, in subthreshold regime, the intrinsic capacitances of DGMOSFET are weakly dependent on the channel length and are very small; therefore, the parasitic capacitances are the dominant component in the effective gate capacitance [3].

We have investigated the effect of Drain/Source Length, thin body thickness and gate underlap, the effective structural parameters on parasitic fringe capacitance, for a device operated in subthreshold regime. In highly scaled devices, (for sub-20nm body thickness), the quantum mechanical effects must be taken in to account [4]. Hence, in our simulations 1-D Schrödinger equation coupled with Poisson’s equation is solved numerically. The solution of the Schrödinger equation was obtained in the direction perpendicular to the Si/SiO\textsubscript{2} interface [5]. In order to compute the effective gate capacitance, AC analysis was used. The rest of the paper is organized as follows. In section 1, we describe the device and its structural parameters. In section 2, we investigate the impact of the structural parameters such as Source/Drain Length, thin body thickness and gate underlap on the electrical characteristics of the device. This section is followed by the conclusion.
1. Device structure

Fig. 1 shows the schematic of simulated DG-SOI MOSFET device. Gate electrodes are made from polysilicon. The effect of depletion in polysilicon is neglected. The gate oxide thickness is equal to 3nm and gate length is 50 nm. Source/Drain regions are n+ with N_D=10^{20} cm^{-3}. Channel is assumed to be made of intrinsic silicon.

![Fig. 1: Schematic of simulated device.](image)

2. The effect of structural parameters on the device characteristics

The C_{Geff} in DGMOS can be expressed as [6]:

\[
C_{G_{eff}} = \text{Series}(C_{ox}, C_{si}) || C_{ov} \parallel C_{if} \parallel C_{of} \quad (1)
\]

Where C_{ox} is the oxide capacitance, C_{si} is the silicon body capacitance, C_{ov} is the gate to Source/Drain overlap capacitance and C_{of} and C_{if} are the outer and inner fringe capacitance. C_{ov} and C_{if} are the parasitic capacitances between gate and Source/Drain through the channel path (C_{id}) and through the insulator path (C_{id}). C_{ov} depends on the overlap length (L_{ov}), channel width (W) and the oxide thickness (T_{ox}). In our device C_{ov}=0 because no overlap exists between gate and Source/Drain. C_{ax} is a function of channel length (L), channel width (W) and oxide thickness. Thus it will become negligibly small in drastically scaled devices. Hence C_{Geff} is predominantly due to fringe capacitances (C_{if},C_{of}). Fringe capacitances strongly depend on the device geometrical dimensions.

2.1 The effect of Source/Drain length:

Fig. 2 shows the effect of Source/Drain length (L_S/L_D) on the I_D(V_{GS}) characteristics. Simulation results are shown only for L_S/L_D equal to 30nm and 250nm. Changes in I_D(V_{GS}) characteristics is negligibly small.

![Fig. 2: the effect of Source/Drain length (L_S/L_D) on the I_D(V_{GS}) characteristics.](image)

This is also confirmed by conduction band diagram in Fig. 3. It is noted that, as the Source/Drain length is decreased, the barrier height will remain approximately constant.

![Fig. 3: the effect of Source/Drain length (L_S/L_D) on the barrier height.](image)

In order to find the gate capacitance an AC analysis was carried out. The gate capacitance was found as a function of L_S/L_D. The results are shown in Fig. 4.

![Fig. 4: gate capacitance as a function of L_S/L_D](image)

It can be seen from this figure that by decreasing L_S/L_D, the C_{Geff} decreases. This is mainly attributed to a decrease in C_{of}. For L_S/L_D values larger than 120nm, the C_{Geff} becomes almost flat. The fringing field lines around the gate and around the Source/Drain regions...
are shown in Fig. 5. Data shown in this figure confirm that the increase in $C_{\text{Geff}}$ is due to the increase in $L_S/L_D$. As $L_S/L_D$ is increased, the fringing field line density reduces to a minimum. Therefore, $C_{\text{Geff}}$ flattens for large $L_S/L_D$ values.

Fig. 5: The fringing field lines around the gate and around the Source/Drain regions for: (a) $L_S=L_D=30 \text{nm}$, (b) $L_S=L_D=250 \text{nm}$.

2.2 The effect of the thin body thickness on the device characteristics:

Thin body thickness ($T_{\text{Body}}$) affects the current voltage characteristics. Fig.6 shows that as the body thickness is decreased the barrier height decreases.

Fig. 6: the effect of body thickness on the barrier height.

As shown in Fig. 7, decreasing $T_{\text{Body}}$ is accompanied by a decrease in the drain current.

Simulations show that as thin body thickness is decreased electron mobility is reduced. This may be attributed to the interface scatterings and explains the reduction in the drain current with decreasing $T_{\text{Body}}$.

The effect of thin body thickness on $C_{\text{Geff}}$ is shown in Fig. 8. $C_{\text{Geff}}$ has been computed in accumulation, depletion and in weak inversion. In latter regime (region of interest for subthreshold operation) the dominant component in $C_{\text{Geff}}$ is the fringing capacitance. Note that, since $C_d$ dose not change with thin body thickness, changes in fringing capacitance in this case is predominantly due to changes in $C_{if}$. Hence, as thin body thickness is reduced $C_{\text{Geff}}$ is increased.

Fig. 8: The effect of body thickness on $C_{\text{Geff}}$

2.3 The effect of Gate underlap on the device characteristics:

In this section the effect of gate underlap on the device characteristics is investigated. In these simulations $L_S$ and $L_D$ as well as the gate length were kept constant.

Fig. 9 shows the effect of different $L_{\text{un}}$ on drain current and Fig. 10 shows the conduction band.
As \( L_{\text{un}} \) is increased, the effect of Source/Drain regions on the channel becomes less pronounced. Therefore relative control of the gate on the channel is increased. This results in an increase in the barrier height and thus a reduction in drain current. As shown in Fig. 11, increasing \( L_{\text{un}} \) reduces the drain induced barrier lowering (DIBL) effect.

Fig. 12 shows \( C_{\text{Geff}} \) as a function of \( L_{\text{un}} \) as obtained from AC analysis. We note that as \( L_{\text{un}} \) is increased, \( C_{\text{Geff}} \) decreases. This characteristic may be used to reduce the delay in the device and is particularly beneficial for low power operation. However the curve \( C_{\text{Geff}}(V_G) \) flattens for large \( L_{\text{un}} \). The distance between \( C_{\text{Geff}}(V_G) \) increases logarithmically as \( L_{\text{un}} \) decreases. This behavior may be explained as follows. From (1) we expect that the dominant component in \( C_{\text{Geff}} \) be the fringing capacitance. However, \( C_{\text{fringe}} \) is a logarithmic function of the underlap [7]:

\[
C_{\text{fringe}} = \frac{K \varepsilon_0 W}{\pi} \frac{\pi W}{\sqrt{L_{\text{un}}^2 + T_{\text{ox}}^2}} \left[ \frac{L_{\text{un}}}{L_{\text{ox}}} \right] \ln \left( \frac{L_{\text{un}}}{L_{\text{ox}}} \right)
\]

This implies that the \( C_{\text{Geff}} \) should be a logarithmic function of \( L_{\text{un}} \).

Fig. 13 shows that an increase in \( L_{\text{un}} \), results in a decrease in the drain current (\( I_D \)). In subthreshold regime \( I_D \) is predominantly due to the diffusion and strongly depends on the barrier height [2].
3. Conclusion

In this paper, we investigated the impact of structural parameters on DG-SOI MOSFET in the subthreshold regime. We have shown that although decreasing Source/Drain length, results in no significant effect on barrier lowering, and on $I_D$, It does significantly increase parasitic capacitance $C_{of}$ and thus $C_{G,eff}$. Decreasing thin body thickness, on the other hand results in a decrease in the drain current and an increase in $C_{G,eff}$. We also observed that as $L_{un}$ is increased, DIBL effect and $C_{G,eff}$ decrease. The results of these studies are useful for design optimization of DGMOS transistor for low power applications.

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REFERENCES


