Implementation of Power Quality Disturbance Classifier in FPGA Employing Wavelet Transform, ANN and Fuzzy Logic

F. Choong*, M. B. I. Reaz**

*Faculty of Engineering, Multimedia University, 63100 Cyberjaya, Malaysia

**Faculty of Engineering, Multimedia University, 63100 Cyberjaya, Malaysia

Abstract: Intelligent power quality monitoring systems have become an essential component of high technology and high availability-oriented industries. Most power quality disturbances are non-stationary and transitory and the detection and classification have proved to be very demanding. The first step towards any solution for a disturbance is to recognize the presence of a particular type of disturbance. This research automates this process where the design and implementation of a power quality disturbance classifier in FPGA is presented. The disturbances of interest include sag, swell, transient, fluctuation, interruption and normal waveform. The approach combines new intelligent system technologies using wavelet transform, artificial neural networks and fuzzy logic and provides some unique advantages regarding fault analysis. The approach developed in VHDL obtained a classification accuracy of 98.17%. The implementation of the project on Altera APEX EP20K200EBC652-1X FPGA utilized 1209 logic cells and achieved a maximum frequency of 263.71 MHz. Experimental results are included to demonstrated the performance of the classifier. The results obtained from the hardware exactly match the results obtained from software simulations when tested with software-generated signals and utility sampled disturbance events. This result validates the utility of the proposed approach.

Key words: Artificial neural network (ANN), classification, discrete wavelet transform (DWT), feature extraction, fuzzy logic (FL), power quality

1 Introduction

The issue of Power Quality is very important to both the consumers and the distributors of electric power. There are many facets of power quality disturbances and each has its own source and mitigation techniques.

Conventional methods for recognition of a power quality disturbance consists of collecting operating data, inspecting the wave forms visually and then identifying any disturbance that may be present in the data. Although the available measuring and recording devices offer substantial help, the process is mainly very slow. Former fault diagnosis algorithms for the transmission systems usually employ FFT and deterministic thresholds. These bring simplicity along with lots of manual works and inaccuracy to the applications.

Neural Networks and Fuzzy Logic Systems are becoming well-recognized tools in PQ capable of perceiving the operating environment and imitating a human operator with high performance. The motivation behind the use of these approaches is based on the complexity of real life systems, ambiguities on sensory information or time varying nature of the system used in PQ. In this respect, neuro-fuzzy control approaches combine architectural (by neural networks) and philosophical (by fuzzy systems) aspects of an expert resulting in an artificial brain, which is to be used as a classifier.

There are a few researches that have been done in this area. In one of the research (Shyh & al., 2002), wavelet transform is employed to detect power system disturbances. This approach unifies time and frequency information and provides an integral signal-processing paradigm, where its embedded wavelet basis serves as a window function to monitor the signal variations very efficiently. The completed prototype is then realized on an FPGA. The second work (Kezunovic & al., 1996), proposes a classification scheme, using a neural network trained to recognize patterns of transmission line faults which is incorporated in a PC-based system, that analyses...
data files from substation digital fault recorders. This system analyses data files coming from the digital fault recorders located in substations. The role of the neural net in this solution is to process current signals and identify the one with the largest disturbance. Furthermore, it will try to classify disturbance according to the fault type. Another work (Jaehak & al., 2002) utilizes a rule-based method and a wavelet packet-based hidden Markov model (HMM) for the classification of power distribution line disturbances. The rule-based method classifies time-characterized-feature disturbances and the wavelet packet-based HMM is utilized for the frequency-characterized feature power disturbances. Lastly, a classifier to carry out waveform recognition in the wavelet domain using multiple neural networks is proposed (Surya & al., 2000). The classifier is able to provide a degree of belief for the identified waveform. The degree of belief gives an indication about the correctness of the decision made. The wavelet-based classifier is equipped with an “acceptance threshold”, which is an agreement level threshold (for the voting scheme), to accept a decision made for the identified waveform.

However, the classification methods employed in the researches mentioned above are based mainly on software implementation. Software simulations are useful for investigating the capabilities of design models and creating new algorithms; but hardware implementations remain essential for taking full advantage of parallelism and provide an increase in speed and performance. Classifiers developed in software have several drawbacks. A limiting factor is that the size of classifier is limited by the size of the system that runs the code for the classifier system. Field Programmable Gate Array (FPGA) does provide a speed-up of several orders of magnitude compared to software simulation (Yasin & al., 2003). This allows all of the system calculations to be done directly in parallel. This contributes a significant increase in performance compared to a systems implemented in software where the many internal calculations compiled into multiple individual commands for a processor to complete sequentially.

A classifier utilizing a combination of all three technologies developed in software was proposed (Huang & al., 2002). In this paper, the authors present a similar classifier but with a different methodology combining the three individual technologies; wavelet transform, neural network and fuzzy logic in hardware resulting in a simpler classifier with a significant increase in speed, performance and accuracy. Important properties and features relevant in determining the type of PQ problem can be extracted using discrete wavelet transform (DWT) and classified using a powerful combination of FL and ANN that result in more robust and accurate classification scheme. The system is then integrated on an FPGA. FPGA was chosen because it greatly reduces the size, offers a higher reliability, improved security, higher performance, higher accuracy and also the ability to add on features easily (Yasin & al., 2003). This research proposes a new fault classification scheme, which hardly needs any interference from users. A hardware classifier allows high operating frequencies with only modest processing power as well as simplified design in hardware and software. The process of PQ assessment is aimed at detecting, classifying and characterizing various power system phenomena affecting PQ. Knowing how and to what extend PQ problems impact sensitive equipment is the most important for users.

2 Design Methodology

Detection of PQ disturbances consists of feature extraction and classification. The procedure adopted to develop a feature-based classifier is as shown in Figure 1.

![Figure 1. Procedures for a feature-based classifier](image)

Simulation of PQ disturbances is performed by third-party tools (Alternative Transient Program (ATP), Matlab and COMTRADE). A total of 10200 examples (1700 examples per class) were collected where the starting time, duration and distortion magnitude are generated randomly. This makes the testing results more reliable because none of these are fixed for real power system disturbance events. Collaboration was made with related parties from Tenaga Research Centre’s PQ Lab. Field data was collected from six different substations from different locations throughout Malaysia includes Bayan Lepas, Bukit Raja, Serdang, Skudai, Telekom Bangsar and TNB Headquarters.
The feature extraction, classification and decision-making process is partitioned into three parts as illustrated in Figure 2.

1. Pre-processing – to extract the disturbance information from the generated power signal.
2. Processing – carry out pattern recognition on the disturbance data.
3. Post-Processing – group the output data and form decisions.

<table>
<thead>
<tr>
<th>Pre-processing</th>
<th>Processing</th>
<th>Post-processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wavelet transform and feature extraction</td>
<td>Neural Networks</td>
<td>Fuzzy Logic</td>
</tr>
<tr>
<td>Disturbance waveform</td>
<td>Disturbance database</td>
<td>Disturbance category and Degree of Belonging</td>
</tr>
</tbody>
</table>

**Figure 2. Block diagram of the automatic disturbance recognition system**

In the waveform generation, six types of disturbances that include transients, sag, swell, interruption, fluctuation and perfect wave are randomly superimposed on the normal waveform at a rate in accordance with their relative occurring frequencies. In this work, the power frequency chosen is 60Hz. The disturbance waveform consists of five cycles of samples of three-phase voltage signals (in per unit).

The samples are fed in as inputs to the pre-processing stage. The pre-processing stage is used to perform feature extraction to extract the disturbance information from the PQ disturbance signal. The disturbance signals are sampled and pre-processed by a 5-level DWT for feature extraction. Since the sampling frequency is set as 256f1 with f1 as the power frequency, the transform coefficients contain the information about the original waveform as shown in Table 1.

**Table 1. Sub-bands of WT coefficients**

<table>
<thead>
<tr>
<th>Transform coefficients</th>
<th>Frequency range</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD1</td>
<td>64f1~128f1</td>
</tr>
<tr>
<td>CD2</td>
<td>32f1~64f1</td>
</tr>
<tr>
<td>CD3</td>
<td>16f1~32f1</td>
</tr>
<tr>
<td>CD4</td>
<td>8f1~16f1</td>
</tr>
<tr>
<td>CD5</td>
<td>4f1~8f1</td>
</tr>
<tr>
<td>CA5</td>
<td>0~4f1</td>
</tr>
</tbody>
</table>

This DWT operation is performed based on equations 1 and 2 respectively:

\[ c_{Ai}(n) = \Sigma k f(n)g_{d}(-k+2n) \]  \[ \text{[1]} \]

\[ c_{Di}(n) = \Sigma k f(n)g_{d}(-k+2n) \]  \[ \text{[2]} \]

The output of the DWT scheme is the feature vectors, i.e., transformed data comprising the approximation coefficients and the detailed coefficients denoted by CA5 and CD1–CD5 respectively representing a particular disturbance signal. Through studying the transform coefficients of variant distorted waveforms, it has been found that each disturbance may only affect one subband coefficient principally.

For example, transient disturbance are “fast changing” signals that have extremely short elapsed time. Therefore, it contains only the spectral contents in the very high frequency range. On the contrary, disturbances such as voltage sag, swell, fluctuation and interruption are “slow changing” disturbances that will affect the lower subband. Figure 3 illustrates the sag detection process where the DWT coefficients carry different types of information of the original waveform in different resolution levels. These coefficients, instead of the original waveforms or the whole transformed data are fed in as pattern inputs to the processing stage to perform pattern recognition and provide an output associated with that pattern. This indicates that WT represent a signal with a few terms and therefore reduce the size of a classifier.

Disturbance classification is the final step of the detection and it is implemented through some form of decision-based system. In this work, a classification method that combines the learning abilities of ANN and the excellent knowledge representation of FL is proposed. The processing stage is made of an ANN block trained to recognize patterns of input/output pair from the disturbance database. The patterns consist of the DWT coefficients as input and the disturbance class is the outputs. The output of the neuron is simply a linear combination of the input vector x with the weight vector mk, as shown in equation 3.

\[ u_{k} = m_{x} = m_{k,i}x_{i} \text{ for } i \text{ from } 1 \text{ to } P \]  \[ \text{[3]} \]

The ANN is trained before it is utilized in the classification process. The algorithm chosen for the ANN implementation was the Univariate randomly optimized Neural Network (uornn) as described by Looney (1997). The algorithm learns to associate successful outputs to the corresponding inputs after repeated learning attempts, through trial and error. Each neuron in the ANN has a “hold_weights” component that does all the interaction with the ANN datapath. This component is composed of two blocks: a storage unit for the weights and the actual neurons. The first block stores the actual weight and eventually stores the new weight values to be tested during training. The second block calculates the output of the whole component. The algorithm loops through the process of generating and testing weights and ends upon obtaining a weight value that produces the least error (Choong & al., 2004).
Finally, the post-processing stage groups the output data and form decisions. This stage is important because the output results from the ANN block may contain some imprecision. Thus, in order to obtain a more accurate result, the output results are then fed into the FL block to further classify the output in one of the six disturbance types based on a set of predefined codeword. A fuzzy classifier consists of three parts, the fuzzification of the inputs, the defuzzification of the outputs and the rule-base. A number of standard rules are used to mimic experienced PQ engineers thought process. The rule-based post processing attempts to correct wrong decisions made by classifiers, thus improves the accuracy of the classification results. FL uses a rule-based reasoning process to analyze PQ data.

![Figure 3. Sag detection process using DWT](image)

In addition, FL allows a system to be more understandable to a non-expert operator. In this way, fuzzy logic is used as a general methodology to incorporate knowledge of PQ to assist in decision-making where the power quality knowledge is presented as a series of rules. A sample rule is as shown below.

**Rule 1:** IF Input1 is High THEN Class is Transient or a high level of input1 often indicates transient.

The two uncertainties to be modeled are “often” and “high”, which are most easily represented as a fuzzy measure and fuzzy set, respectively. The crisp output is determined using equation 4.

$$\text{Output} = \frac{\sum \text{fuzzy output} \times \text{singleton}}{\sum \text{fuzzy output}}$$

The NN was used to fine tune and refine the FL system, adjusting rules as the system is running. The rule-based post-processing improves the accuracy of the classification result.

The system presented in this work is designed to recognize six types of PQ disturbances. These disturbances are identified by taking readings of the voltage values (in per unit) of each cycle in the time domain. The values are then compared against the preset characteristic of a particular PQ disturbance as defined by the IEEE 1159.2 working group. The voltage values (in per unit) are then fed into the DWT block to obtain the coefficient values that carries the disturbance information of the original PQ disturbance signal. The ANN is trained with these coefficients covering samples of disturbance data from each class. Fuzzy rules were established to perform the classification task. Using the same principles, the classification of other types of PQ disturbances such as capacitor switching, notching, impulse, etc. can be easily achieved.

### 3 Hardware Implementation

The implementation of the entire system on EP2K200EBC652-1X of APEX20KE family (an ALTERA FPGA) is described in this section. The APEX DSP development board (Altera Corporation, 2000) features the APEX20KE device in a 652-pin package. In this project, this prototyping board was used to debug and verify both the functionality and design timing. The EP2K200EBC652-1X device features 211,000 gates in a 652-pin FineLine BGA™ package. The device has 8,320 logic cells and 106,496 RAM bits.

The whole design is described using IEEE-compliant VHDL language. VHDL is the abbreviation for VHSIC hardware description language while VHSIC is an abbreviation for Very High Speed Integrated Circuit. Hardware Description Languages (HDL) was developed to describe how hardware behaves. Altera Multiple Array MatriX Programmable Logic User System (hereinafter referred to as Max+PlusII) version 10.2 and Quartus II version 4.0 (Altera Corporation, 1997) are the software that were used in the coding, design, compilation and testing of
The synthesis report generated by Quartus II version 4.0 after successfully synthesizing the project summarizes the hardware utilization of the project. The project utilized a total of 1209 logic gates and 73 input/output pins on the EP20K200EBC652-1X device. The timing analyser tool provided timing specifications for the project. The maximum frequency (Fmax) achieved is 263.71MHz.

The set-up for the project is as shown in Figures 4. The Altera DSP Development board is connected to a laptop using an Altera byteblaster download cable. A pattern generator is used to generate FPGA input label signals and feed them into the chip and capture signals from these chip’s output by using a logic analyzer. This verification model reflects the real responses not only from virtual simulation by software, but it is also a real chip working result. Both the pattern generator and logic analyzer mainframes are connected to a laptop.

This is done using a USB cable. All the three devices are then connected together using signal connectors, ground lines, probes and jumper wires.

4 Results and Discussions

The results of classification using simulated and real data set for all six disturbances are shown in Table 2. The table is organized as follows: in each row the performance of the network is represented by a specific PQ disturbance type, each column represents the results of the classification. The percentage of correct classification is calculated using equation 3.

\[
\% \text{ correct classification rate} = \frac{\text{Total correct classified disturbance events}}{\text{total disturbance events}} \quad [5]
\]

<table>
<thead>
<tr>
<th>C</th>
<th>Correct</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>97.24</td>
<td>-</td>
<td>0.6</td>
<td>0.8</td>
<td>-</td>
<td>1.1</td>
<td>0.26</td>
</tr>
<tr>
<td>2</td>
<td>97.14</td>
<td>1.15</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>1.26</td>
<td>0.35</td>
</tr>
<tr>
<td>3</td>
<td>98.87</td>
<td>0.4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.73</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>98.20</td>
<td>0.03</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.54</td>
<td>0.23</td>
</tr>
<tr>
<td>5</td>
<td>97.73</td>
<td>1.27</td>
<td>0.2</td>
<td>0.8</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>99.98</td>
<td>-</td>
<td>0.01</td>
<td>0.01</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Testbenches were used to perform extensive testing on each individual component. Performance on
the test set reached an average of 98.17% accuracy. The combination of WT and ANN produced a classification accuracy of 96.17%. The accuracy of the proposed method without FPGA integration is 98.05% by performing functional simulation, which differs from the overall classification accuracy (98.17%) by 0.12%. The overall classification accuracy is obtained by performing timing simulation. This proved the feasibility and efficiency of the proposed classifier that integrates all the three methods using FPGA.

Due to space constraint, the classification results of two types of power quality disturbances are shown in Figures 5 to 6. Two possible operation modes exist: training mode and evaluation mode controlled by Train_Eva. Evaluation mode is selected when Train_Eva='1'. Op_select enables the option to train, output weights, load weights and evaluate. An option of ‘1002=4H’ activates the loading of final weight values to the respective neurons followed by ‘1012=5H’ that enables the classification process to take place. The system obtains input values from Input_ADC consisting of disturbance data and fed in as inputs to the DWT. The DWT processes and extracts features from the data set. The ANN then performs pattern matching on these features and final classification by the FL. The type of disturbance and the degree of belonging to the disturbance class are indicated by disturbance_type and Output respectively. The Sig signal synchronizes the operation of all the blocks that make up the system. The Reset signal resets the settings of the DWT block. The En_ADC signal enables the ANN to accept input signals from the Input_ADC, The Ck signal activates the system. The send_frame signal indicates that the output is available on the dataout register. The dataout register holds the output results. Lastly, the data_train provides instructions to the ANN block to perform a specific operation.

In order to classify the six disturbances, individual codeword is predefined and assigned to each class. An output of “001” on the result register represents a transient disturbance, “010” represents a sag, “011” represents a normal waveform, “100” represents a swell, “101” represents an interruption and “110” represents fluctuation. Logic analyzer captures the results obtained from Altera EP20K200EB652-1X FPGA as shown in figures 7 to 8. Labels disturbance_type indicates the type of disturbance, send frame indicates that the results are ready on the output register and output indicates the degree of belonging to the particular disturbance class. An output of “010” represents a sag and “100” represents a swell. The results obtained exactly matched the results obtained from software simulations.

Figure 5. Classification Results for Voltage Sag
Figure 6. Classification Results for Voltage Swell

Figure 7. Final classification of voltage sag disturbance class
5 Performance Comparisons

5.1 Comparison Between Software and Hardware Implementation

The main objective of this section is to present a summary of the results obtained from software simulations and hardware implementation in order to determine the effectiveness of the proposed method. Table 3 presents results comparison between the two approaches. Based on the results obtained, it can be concluded that the results obtained from the hardware exactly matched the results obtained from software simulations. In both cases, the system worked as expected and successfully classified all six PQ disturbances types.

<table>
<thead>
<tr>
<th>Disturbance Type</th>
<th>Software Simulation</th>
<th>Hardware Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient</td>
<td>001</td>
<td>001</td>
</tr>
<tr>
<td>Sag</td>
<td>002</td>
<td>002</td>
</tr>
<tr>
<td>Normal</td>
<td>003</td>
<td>003</td>
</tr>
<tr>
<td>Swell</td>
<td>004</td>
<td>004</td>
</tr>
<tr>
<td>Interruption</td>
<td>005</td>
<td>005</td>
</tr>
<tr>
<td>Fluctuation</td>
<td>006</td>
<td>006</td>
</tr>
</tbody>
</table>

5.2 Hardware Implementation Alternatives

In regard to the designated hardware of FPGA realization, Table 4 lists the implementation performance using a few selected devices. In optimizing the design, a balance between frequency and area was taken into account to select a suitable device. The project was successfully synthesized using APEX20KE EP20K200EBC652-1X device family from Altera Corporation as it utilizes the lowest area and offers the highest frequency.

<table>
<thead>
<tr>
<th>Family</th>
<th>Device</th>
<th>Area</th>
<th>Fmax</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apex</td>
<td>EP20K200CQ240C7</td>
<td>1545/8320</td>
<td>84.57  MHz</td>
</tr>
<tr>
<td>ApexII</td>
<td>EP2A25B724C7</td>
<td>1545/24320</td>
<td>85.47  MHz</td>
</tr>
<tr>
<td>Flex</td>
<td>EPF10K50SBC365-1</td>
<td>1559/2880</td>
<td>55.56  MHz</td>
</tr>
<tr>
<td>Mercury</td>
<td>EP1M120F484C5</td>
<td>1432/4800</td>
<td>121.95 MHz</td>
</tr>
<tr>
<td>APEX</td>
<td>EP2K200EBC652-1X</td>
<td>1209/8320</td>
<td>263.71 MHz</td>
</tr>
</tbody>
</table>

5.3 Comparison Among Related Works

5.3.1 Simulation Results

In order to examine and analyze the effectiveness and feasibility of the proposed approach, a comparison in terms of percentage of accuracy is made and presented in Table 5. Method by Jaehak & al. (2002), employing wavelet and fuzzy to classify PQ disturbances produced the highest result, followed by the proposed method in this paper employing neural network, fuzzy logic and wavelet transform, followed by method by Huang & al. (2002) employing wavelet transform and neural fuzzy to detect PQ disturbances, followed by method by Kezunovic & al. (1998), detecting and classifying faults using neural network and finally, PQ disturbance waveform recognition employing wavelet and neural network method by Surya & al. (2000). From Table 5,
it can be concluded that a combination of more than one method yields a better result.

<table>
<thead>
<tr>
<th>Table 5. Performance comparisons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method</td>
</tr>
<tr>
<td>Wavelet Transform and Neural Fuzzy (Huang et al, 2002)</td>
</tr>
<tr>
<td>Wavelet-based Neural Classifier (Surya et al, 2000)</td>
</tr>
<tr>
<td>Proposed Method</td>
</tr>
<tr>
<td>Neural Network (Mladen et al, 1996)</td>
</tr>
<tr>
<td>Wavelet and Fuzzy Logic (Jaehak et al, 2002)</td>
</tr>
</tbody>
</table>

Method by Jaehak & al. (2002) yielded the highest result. However, the response time of a fuzzy based classifier for classifying disturbance signals slows down as the number of rules grows larger. It also takes time to refine the rules and membership values. This limitation is found in similar works in fuzzy logic by Dash & al. (2000) and Kezunovic & al. (1998), where the classification time taken is 0.02 seconds and 15 milliseconds respectively. In comparison, this work yields a shorter classification time of 16 microseconds using the same data set. This shows that limitations exist for software implementation in which they will never be fast enough compared to hardware platforms.

It is also observed that all the methods above are based mainly on software implementation. Often, many practical applications including PQ require a large computational power to cope with complexity or real-time constraints. Often such power is not available from traditional computers, or it is too expensive and cannot always be afforded. In addition, software implementation must run on computers or large machines and this require the existence of these machines that pose a constraint on space and make a classifier system less portable. On the other hand, hardware implementations already provide, for many applications, adequate power and gates in a single chip package (John & al, 1995).

It is clear that, the proposed method eliminates the limitations mentioned above. The performance of the classifier is encouraging. The results reveal that the proposed approach is computationally simple, accurate and exhibits a good balance between flexibility, speed, size and design cycle time. These important characteristics are needed to design a good classification system (Sanchez, 1997). Comparison and results presented validate the successful classification of PQ disturbance.

Based on the comparisons made above, the feasibility and useful features of the new approach are further summarized and justified as follows:

1. For feature extraction, the proposed method uses DWT that enables signal representation with a few terms and can effectively remove redundancy of time domain data and therefore reduce the size and complexity of the classifier.
2. For the classification method, the proposed method combines the learning abilities of ANN and the excellent knowledge representation of fuzzy logic. This produced a more intelligent system, with recognition performance better than those obtained by the individual technologies.
3. ANN is used for its pattern recognition capabilities. However, its ability to perform well is greatly influenced by the weight adaptation algorithm. Thus a unique algorithm, uronn was chosen for implementation of neural network. This algorithm is a very advantageous approach in the implementation of a neural network as explained earlier as it simplifies calculation, minimizes error, reduces training time and provide a significant increase in the accuracy of the classification (Looney, 1997).
4. As there exists uncertainty in the training set and in the subsequent pattern recognition, FL is used to determine the final output rather than taking the output of the neural network as the final classification, improving robustness in the system and producing a more accurate result.
5. The VHDL model provides a systematic approach for hardware realization, facilitating the rapid prototyping of wavelet transform, neural network and fuzzy logic for power system applications.
6. A hardware implementation using FPGA could take advantage of the high speeds achievable using hardware, and as a result the design would be a beneficial and economic investment.
7. The system owns the potential of being extended to classify other kinds of PQ disturbances.
8. This novel combination of methods shows promise for further development of a fully automated PQ monitoring system.
9. The combination of the wavelet transform, neural network and fuzzy logic achieves outstanding performance in the ability to adapt to various power quality phenomena. Without any structure modification, the scheme can be easily applied to other types of power quality disturbances.
10. The ability to reconfigure the FPGA, as requirements change in future projects, avoids product obsolescence and extends product life cycles (Nigel & al, 2001).

5.3.2 Synthesis Results

In one of the work by Shyh & al (2002), the wavelet transform circuit is made through two FPGA chips, which are XC4010XL IC developed by Xilinx, Inc. The maximum frequency achieved is 80 MHz. The total number of logic cells utilized in the two FPGA chips is 8184 and 8160 respectively. In comparison, this method utilized only 1432 logic cells and could run at a frequency of up to 121.95 MHz. The proposed method exhibits a good balance between area and frequency, which is vital in any hardware design.
Conclusion

A new approach of hardware prototyping for the realization of PQ disturbance classifier utilizing wavelet transform, neural network and fuzzy logic is proposed. The initial work involved determining the functions of the system and designing the individual modules in VHDL. The functionality and timing behaviour of the modules were successfully verified. Finally, the system was synthesized to the Mercury EP1M120F484C5 FPGA device. The performance of the classifier is encouraging. The results reveal that the proposed approach is computationally simple, accurate and exhibits a good balance of flexibility, speed, size and design cycle time. These important characteristics are needed to design a good classification system. Comparison and results presented validate the successful classification of PQ disturbance.

Acknowledgment

The authors would like to express great appreciation to the funding resource that supported this work. This work was supported by Intensified Research in Priority Areas (IRPA), a Ministry of Science & Technology Malaysia sponsored program for the advancement of R&D activities. The project no is 03-99-01-0074-EA071. The authors also wish to thank Tenaga Nasional Research and Development Centre for providing valuable assistance in obtaining power disturbance field data from the various substations throughout the country.

References