Transient Analysis of Bang-Bang Phase locked Loops without Cycle Slipping for Frequency Step Inputs

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Abstract— In this paper an exact transient analysis of Bang-Bang PLLs (BBPLLs), as a nonlinear system, is presented. The proposed analysis considers the input step in frequency. The results contain all important times, the related VCO control voltage and output excess phase. We considered frequency steps in which BBPLL does not experience cycle slipping. We could obtain an expression for maximum frequency step size in which cycle slipping does not occur. To evaluate the proposed analysis, many simulations are performed using MATLAB SIMULINK where all show very high accuracy of the proposed equations.

Keywords- BBPLL; Nonlinear; Operation; Transient analysis

I. INTRODUCTION

Since the modern clock and data recovery (CDR) architectures often rely on phase locked loop circuits to extract timing information from incoming data signals, the use of bang-bang phase locked loops has become increasingly common in a lot of communication systems, especially in CDR system. The main application of BBPLLs is in high speed systems where minimum pulse widths relative to bit periods and power considerations cause problem in recovery of data signals. These systems use a bang-bang phase detector (BBPD) in the loop, which samples data as a part of the phase detection process, therefore there exists no systematic phase error between the data signals and the recovered clock signals. BBPD quantizes the phase error between input (data) and output (clock) with 1-bit resolution.

Unfortunately, transition-sampling flip-flop-based phase detectors can provide only binary (early/late) or ternary (early/late + hold) phase information [2]. This amounts to a hard non-linearity in the loop structure, leading to an oscillatory steady-state and rendering the circuit unanalyzable with standard linear PLL theory [6]. This behavior of the BBPLLs causes that the researchers make effort to analyze it.

BBPLL circuits must satisfy some specifications such as capture range, locking time and jitter performance in lock, posing challenges to circuit and system designers. Most researches focused on jitter and noise analysis (see [04][72]) but there exists a few researches on the transient analysis. Design of the BBPLL in higher speeds is the most important reason to analyze the BBPLL in time domain. Transient behavior of a BBPLL in response to the phase and frequency step inputs is a main issue in time domain that this paper has focused on frequency step response in which BBPLL does not see cycle slipping. Because of the nonlinear behavior of the BBPLL, these inputs cause responses with two different general forms depending on the input step size. In multi rate systems, the analysis of transient behavior in frequency step inputs is very important. Cycle slipping is the phenomenon that occurs for large frequency step sizes and makes the response different from that of the small step sizes [11]. In the small step cases, the phase error never reaches $\pi$ or $-\pi$. It is obvious that BBPLL under cycle slipping is in more unstable and noisy. Therefore, design of BBPLL which never experience cycle slipping can be beneficial. Unfortunately there are few researches on transient analysis of BBPLL. Only paper [11] considers cycle slipping in an approximate analysis in which the calculated locking time is for large frequency step sizes. This makes us to investigate the transient analysis of BBPLL which never experiences cycle slipping. This makes us able to design BBPLL with higher speed. The rest of the paper is as follows: Section 1 introduces BBPLL with first order loop filter and the mathematical principles governing on the BBPLL. In section 2 the proposed transient analysis and a new technique are presented to obtain all important times and the related VCO control voltage and output excess phase where cycle slipping does not occur. Also an expression for maximum frequency step size in which BBPLL does not experience cycle slipping is presented in this section. Simulation results, showing the validity of this method are presented in section 3. Finally, section 4 gives conclusions.

Fig 1. BBPLL architecture with first order filter
II. BANG-BANG PLL MODEL

Consider two cases of BBPLL: BBPLL with zero order and first order filters. References [2] and [MCH 11] have illustrated the operation of these two PLLs clearly. The operation of the BBPLL with zero order filters is straightforward and unremarkable. Due to the low speed and small capture range of the BBPLLs with zero order filter, their use is forward and unremarkable. Due to the low speed and small operation of the BBPLL with zero order filter is straightforward and unremarkable. Due to the low speed and small capture range of the BBPLLs with zero order filter, their use is very limited [2]. In contrary, the BBPLL with first order filter is noticeable. Fig 1 shows a BBPLL with first order filter. This structure adds an integral path to the loop filter of the system. This integral path provides bigger capture range and makes the loop faster. Because of these compelling advantages, the bang-bang loop with first order filter has become a common design choice for state-of-the CDR designs. For this reason, in this paper, we have focused on the BBPLL with first order loop filter used as a CDR. Consider a BBPLL with first order filter shown in Fig 1. The BBPLL consists of a bang-bang phase detector, charge pump with current \( I_p \), a first order loop filter with resistance \( R_p \) and capacitor \( C_p \) connected in series, and voltage controlled oscillator (VCO) with gain of \( K_{VCO} \). In a BBPD a binary error signal is generated in response to phase differences between the input (data) and the output (clock) signals. This binary error signal determines whether the input phase is early or late with respect to the output phase. This characteristic of BBPD can inherently lead to higher charge pump activity, possibly increasing the output jitter [5]. Positive pulses at the output of the phase detector mean that the phase error is positive. Similarly negative pulses mean that the phase error is negative.

![Fig 3. Data (input) signal with frequency of \( \omega_i / 2 \) and clock (output) signal with frequency of \( \omega_o \)](image)

The output voltage of the BBPD, \( v_{pd} (t) \), is a binary form of voltage as \( \text{sign}(\varphi_{in} (t) - \varphi_{out} (t)) \) where it has indication of the sign of phase error between the input (data) and the output (clock) (Fig 2). The parameters \( \varphi_{in} (t) \) and \( \varphi_{out} (t) \) refer to the phase of PLL input (data) and output (clock) signal respectively. \( v_{pd} (t) \) can be shown as (1).

\[
v_{pd} (t) = \text{sign} (\varphi_{in} (t) - \varphi_{out} (t))
\]  

(1)

Control voltage of VCO can be written as (2) by analyzing Fig 1.

\[
v_{cvo} (t) = R_p I_p (t) + \int \frac{I_p (t)}{C_p} dt
\]

\[
I_p (t) = I_p \times v_{pd} (t) = \pm I_p \Rightarrow v_{cvo} (t) = \pm R_p I_p \pm \frac{I_p}{C_p} t
\]

(2)

VCO used in Fig 1 has been assumed linear and the related equation is considered as follows:

\[
\omega_{out} (t) = \omega_i + k_{VCO} v_{cvo} (t)
\]

(3)

Where \( \omega_{out} (t) \) is frequency of VCO and \( \omega_i \) is input frequency. In the BBPLL based CDR, with the input data signal shown in Fig 3, in the steady state condition the output phase (frequency) is twice of the input phase (frequency) [1]. So when the input phase (frequency) changes from its steady state condition, the PLL experiences a transient time and the output phase (frequency) reaches to a new steady state; twice of the input new phase (frequency). So in locked condition, the output phase (frequency) is twice of the input (data). So in locked condition at the VCO central frequency \( \omega_i \) (nominal condition), we consider the input frequency equal to \( \omega_i / 2 \) in equations governing on the BBPLL. According to what illustrated in [12], we can express the input and output phases as (4) and (5) in response to input frequency step, \( \Delta \omega_i \).

\[
\varphi_{in} (t) = \int \left( \frac{\omega_i}{2} + \Delta \omega_i (t) \right) dt = \frac{\omega_i}{2} t + \Delta \omega_i t
\]

(4)

\[
\varphi_{out} (t) = \int \omega_{out} (t) dt = \omega_i t + K_{VCO} \int v_{cvo} (t) dt
\]

(5)

![Fig 4. Variations of output and input excess phase in response to input frequency step](image)
refers to the average frequency error of the t
So excess phase error is written as t
and corresponds to a positive frequency step occurs at (8) t
investigated and verified using simple simulations. Fig 4 shows the output excess phase (ϕ = ϕ
Since at the nominal steady state, the phase error, Fig 5.
As we know, in the locked condition, the output frequency is twice of the input. Using this point along with equation (7), (6) should be rewritten as (8).

After locking, as mentioned above, the output phase is twice of the input, so according to (4) and (5), we have (7).

As we know, in the locked condition, the output frequency is twice of the input. Using this point along with equation (7), (6) should be rewritten as (8).

Or we can consider a factor of 1/2 for output excess phase ($K_{vco} \int v_{\text{out}}(t) dt$) instead of factor of 2 for input excess phase ($\Delta \omega t$) in equation (8). Equation (8) guarantees that $\varphi_e(t) = 0$ is equal to the locked condition. This also can be investigated and verified using simple simulations. Fig 4 shows the output excess phase ($K_{vco} \int v_{\text{out}}(t) dt$) along with the input excess phase ($2 \Delta \omega t$) in response to input frequency step. The frequency step appears as a ramp function in phase. Fig 4 shows the transient of the system where the system finally locks and in the locked times the output excess phase is twice of input excess phase. Note that in BBPLL, this is interpreted as locked condition with zero phase error. Using this point, we can obtain the VCO control voltage in steady state as (9).

\[ \varphi_e(t) = 2 \Delta \omega t - k_{vco} \int v_{\text{out}}(t) dt = 0 \]

\[ \Rightarrow v_{\text{out,steady}} = \frac{2 \Delta \omega}{K_{vco}} \]

The voltage presented in (9) is exactly the same as what simulations show. This model is the same as BBPLL model discussed in [4]. As mentioned above, the purpose of this paper is to derive the all information of the transient time. At first, the previous works are briefly discussed. Reference [11] studied the transient behavior of the BBPLL with first order filter where BBPLL experiences cycle slipping. The analysis has an approximate approach. The derived equation for the locking time was presented as (10).

\[ t = \frac{1}{2 \Delta \varphi \alpha K_{vco} \ln \left( \frac{1 - 2 \Delta f_{ave} T}{1 - 2 \Delta f_{ave} f} \right)} \]

In (10) $\Delta \varphi$ is the change of the phase error contributed by both the integral ($\alpha = I_{pd} / C_{vco}$) and the proportional loop gain ($\beta = I_{pd} R_p$), $f_{ave}$ refers to the average frequency error of the system over a given cycle slipping period, $f_o$ corresponds to initial frequency error (when time equals zero) and $T$ refers to the update period of output signal of VCO [11]. Reference [11] focused on cycle slipping. In this paper we obtain many critical points, such as rise time, peak time and overshoot, etc, for which BBPLL does not enter in cycle slipping.

The next section introduces the proposed analysis.

III. PROPOSED TRANSIENT ANALYSIS

To derive the related equations for transient behavior of the BBPLL without cycle slipping, we have to analyze the system for the frequency step sizes that BBPLL doesn’t experience cycle slipping.

A. Transient analysis of BBPLL without cycle slipping

Fig 5 shows the control voltage ($v_{\text{out}}(t)$) and excess phase error ($\varphi_e(t)$) in response to the input frequency step in which BBPLL does not experience cycle slipping. In a BBPLL, when a positive frequency step occurs, the phase and frequency errors are large at the beginning, after some time decrease and gradually reach zero. So the number of positive pulses generated at the beginning is much more than the next times while BBPLL is locking. As Fig 5 shows, BBPLL is in steady state and suddenly at $t = 0$ a positive frequency step occurs at the input. Regarding to $v_{\text{out}}(t) = \text{sign}(\varphi_{in}(t) - \varphi_{out}(t))$, the phase detector senses positive phase error and produces positive pulses (Fig 6) and charges the loop filter and increases the voltage control; consequently the phase error reaches zero but the output frequency isn’t twice of the input yet, this is not the locked condition, so phase error switches toward negative values, this happens at the time $t = t_1$, after a time interval the
Fig 6. Phase detector output along with excess phase error (\(\varphi_e(t)\)) in response to positive small frequency step.

Phase error again back to positive values and this is repeated iteratively and finally at a time the BBPLL locks. At this time the output frequency is twice of the input. The equations obtained in (2) and (8) verify this transient behavior too. As shown in Fig 5, phase error reaches zero having three crossing points. How much BBPLL gets toward lock point, the number of positive and negative pulses in successive intervals decreases. So the first peak in the phase error, \(\varphi_{e,max}\), is the biggest one in the transient intervals (Fig 5, 6). Fig 6 shows the phase detector output \(v_{pd}(t)\) along with phase error. It simply shows the decreasing of the number of pulses, as expected. As shown in Fig 5, the first peak of control voltage is \(v_{cot}\) that occurs at \(t = t_1\). Important times \(t_1, t_2, t_3, \ldots t_n\) along with their related amplitude in control voltages: \(v_{cot,1}, v_{cot,2}, v_{cot,3}, \ldots, v_{cot,n}\) have been shown in Fig 5, \(n\) is the number of time intervals that the phase detector output switches from positive pulses to negative pulses and vice versa, here in Fig 5, \(n\) equals 3. We obtained that the control voltage of VCO can be expressed as (2). Substituting (2) into (8) the excess phase error in the system is obtained as (11).

\[
\varphi_e(t) = 2\Delta\omega - (\pm R_p I_p \kappa_{cot} t + \frac{K_{cot} I_p}{2C_p} t^2) 
\]

The transient behavior of (11) is exactly the same as what presented in Fig 5 and Fig 6. Regarding to the different intervals of transient, one of the signs + or – may be valid in (2) and (11), the plus and minus signs are considered for positive and negative pulses respectively. To calculate the important points, we firstly consider the times that phase error becomes zero. The peaks of voltage control are occurred at these zero crossing times, because at these times phase detector changes the sign of pulses it generates (Fig 5, 6). To calculate \(t_1\), we have:

\[
\varphi_e(t) = 2\Delta\omega - R_p I_p \kappa_{cot} t + \frac{K_{cot} I_p}{2C_p} t^2 = 0
\]

\[
\Rightarrow t_1 = t_p = \left(\frac{4\Delta\omega C_p}{I_p K_{cot}} - 2R_p C_p\right)
\]

\(t_1\) is the first time interval that phase error reaches to zero. Since the first interval, \(t_1\), contains the maximum number of positive pulses, \(t_1\) is the peak time (\(t_p\)) of control voltage and the first peak of control voltage, \(v_{cot, max}\) occurs for \(t = t_1\) and is calculated as (13) by substituting (12) into (2). Note that in the first interval, the pulses are positive, so the sign of (2) has to be positive.

\[
v_{cot,1} = v_{cot, max} = \frac{4\Delta\omega}{K_{cot} - \frac{I_p R_p}{2}}
\]

As mentioned, this is the maximum voltage that VCO experiences in the transient region. So this value of voltage can be a criterion for overshoot of the control voltage. Equation (13) shows, the maximum voltage of VCO is an increasing function of the frequency step size and also is a function of circuit parameters. Note that the first jump of control voltage, \(v_{cot,1}\), at \(t = 0\), at the beginning of positive frequency step is \(+R_p I_p\) (Fig 5). As mentioned before, the maximum phase error occurs in this interval too. So we find the maximum phase error (\(\varphi_{e,max}\)) and the related time \((t_{p, phase})\) using (11) as below.

\[
\frac{d\varphi_e(t)}{dt} = 2\Delta\omega - R_p I_p \kappa_{cot} t - \frac{K_{cot} I_p}{2C_p} t^2 = 0
\]

\[
\Rightarrow t_{p, phase} = \frac{2\Delta\omega C_p}{K_{cot} I_p R_p} - R_p C_p
\]

At the time \(t = t_1\) (the first zero crossing point in phase error), the phase error starts becoming negative and consequently negative pulses are generated so that current jumps switches from \(+I_p\) to \(-I_p\). So control voltage experiences a jump of size \(-2R_p I_p\) and capacitor starts discharging and control voltage decreases (Fig 5). So for the second interval \((t = t_2)\) we can write (15) for control voltage. It is obvious that at the next period of positive pulses, the voltage jumps is \(+2R_p I_p\) (see time interval, \(t_3\), in Fig 5).

\[
v_{cot}(t) = -2R_p I_p \frac{t}{C_p} + v_{cot,1}
\]

In (15), \(v_{cot,1}\) is the peak of control voltage at \(t = t_1\). Similarly substituting (15) into (8), the excess phase error in second time interval can be written as (16)

\[
\varphi_e(t) = 2\Delta\omega + 2R_p I_p \kappa_{cot} t + \frac{K_{cot} I_p}{2C_p} t^2 - K_{cot} v_{cot,1} t
\]

To calculate the second peak of voltage, first we calculate the second time interval \((t = t_2)\), in second zero crossing point of excess phase error, so we have:
\[ \Rightarrow t_2 = \left( \frac{4 \Delta \omega C_p}{I_p K_{vcx}} - 6 R_p C_p \right) \] (17)

The second peak in control voltage is obtained as (18) by substituting (17) into (15).

\[ v_{cot,2} = 3R_p I_p \] (18)

Continuing this process to find the peaks of control voltage and related times, we reach to the following general recursive equations. For the time interval with positive pulses (odd \( n \)) the recursive equation of (19) holds for peaks of control voltage.

\[ v_{cot,n} = +2R_p I_p + \frac{I_p}{C_p} t_n + v_{cot,(n-1)} \quad \text{odd } n \] (19)

For the related time, \( t_n \) (zero crossing intervals in excess phase error) substituting (19) into (8), we have:

\[ t_n = \frac{2\Delta\omega - 2R_p I_p K_{vcx} - K_{vcx} v_{cot,(n-1)}}{K_{vcx} I_p} 2n \quad \text{odd } n \] (20)

Having \( t_n \), the recursive equation of peaks in control voltage mentioned in (19) is finally rewritten as (21) by substituting (20) into (19).

\[ v_{cot,n} = \frac{4\Delta\omega}{K_{vcx}} - 2R_p I_p + v_{cot,(n-1)} \quad \text{odd } n \] (21)

Note that we have a positive step input, so phase detector generates positive pulses and in a similar way we will have:

\[ t_n = -\frac{2\Delta\omega - 2R_p I_p K_{vcx} + K_{vcx} v_{cot,(n-1)}}{K_{vcx} I_p} 2n \quad \text{even } n \] (22)

And the related peak in control voltage will be as (23).

\[ v_{cot,n} = -\frac{4\Delta\omega}{K_{vcx}} v_{cot,(n-1)} \quad \text{even } n \] (23)

Since we have time intervals from (20) and (22), we can simply find the all-time intervals as follows:

\[
\begin{aligned}
 t_1 &= \left( \frac{4\Delta\omega C_p}{I_p K_{vcx}} - 2R_p C_p \right) \\
 t_2 &= \left( \frac{4 \Delta \omega C_p}{I_p K_{vcx}} - 6 R_p C_p \right) \\
 t_3 &= \left( \frac{4 \Delta \omega C_p}{I_p K_{vcx}} - 10 R_p C_p \right) \\
 &\vdots
\end{aligned}
\] (24)

We can simply show that the above expressions for all \( n \) can be expressed as a unique general equation as (25). It is seen that (25) is not a recursive equation.

\[ t_n = \frac{4\Delta\omega C_p}{I_p K_{vcx}} - (4n - 2)R_p C_p \quad \text{each } n \] (25)

Similarly, having (21), the peaks of the control voltage in odd intervals are given as follows:

\[
\begin{aligned}
 v_{cot,1} &= \frac{4\Delta\omega}{K_{vcx}} I_p R_p \\
 v_{cot,3} &= \frac{4\Delta\omega}{K_{vcx}} - 5I_p R_p \\
 v_{cot,5} &= \frac{4\Delta\omega}{K_{vcx}} - 9I_p R_p \\
 &\vdots
\end{aligned}
\] (26)

Finally for even \( n \), the peaks of the control voltage are obtained as follows:

\[
\begin{aligned}
 v_{cot,2} &= 3I_p R_p \\
 v_{cot,4} &= 7I_p R_p \\
 v_{cot,6} &= 11I_p R_p \\
 &\vdots
\end{aligned}
\] (28)

Similarly above equations can be expressed generally as (29).

\[ v_{cot,n} = \frac{4\Delta\omega}{K_{vcx}} -(2n - 1)I_p R_p \quad \text{even } n \] (29)

It is seen that the obtained equations (27)-(29) for \( v_{cot,n} \) are not recursive. Thus we could obtain all time intervals and peaks of voltage in transient time when input frequency step size is small. Now we can give some overall performance measures that are common in transient analysis, like rise time, locking time. One of the most important times in transient time is the locking time, \( t_s \), that it is equal to sum of the all-time intervals calculated by (25), as (30).

\[ t_s = t_1 + t_2 + t_3 + \ldots + t_n \] (30)

To find \( n \), note that all times obtained from (26) should be positive, this make us able to find the upper bound for \( n \) and regarding to the integer nature of \( n \), we have

\[ t_n = \frac{4\Delta\omega C_p}{I_p K_{vcx}} -(4n - 2)R_p C_p > 0 \] (31)

\[ n = \left[ \frac{\Delta\omega}{I_p R_p K_{vcx}} + \frac{1}{2} \right] \]

Since the locking time depends on \( n \) and so \( n \) can be somehow a criterion of speed of the system. Therefore smaller \( n \) can be corresponding to the higher speed BBPLL.

One of the other most important times in transient region of the BBPLL is the rise time \( t_{rise} \) which is the first time that the control voltage reaches to its final value (see Fig 5). We simply find the time in the first interval that control voltage firstly reaches to steady state value \( (2\Delta\omega/K_{vcx}) \), so we have:

\[ t_{rise} = \frac{4\Delta\omega C_p}{I_p K_{vcx}} - 2R_p C_p \]
\[ v_{out}(t) = +R_p I_p + \frac{I_p}{C_p} - \frac{2\Delta \omega}{K_{vco}} \]
\[ \Rightarrow t_{rise} = \frac{2\Delta \omega C}{I_p K_{vco}} - R_p C_p \] (32)

As Fig 6 shows, contrary to linear PLL, in the steady state, there are consecutive up and down pulses at phase detector output [13]. Because of the resistor, the control voltage experiences positive and negative jumps from the final value \(2\Delta \omega/K_{vco}\) (see the locked region in Fig 5). This phenomenon causes ripple on the control line of VCO in the steady state and does not depend on input size. Here our focus is on the transient analysis, so features like these can be investigated as a distinct steady state analysis [13].

Deriving the above closed form equations, we have completed the transient analysis for frequency step, indeed we analyzed the BBPLL when cycle slipping doesn’t occur and the all-important times of transient region have been derived.

### B. Maximum frequency step without cycle slipping

As mentioned in section A, in frequency steps where cycle slipping does occur, phase error never reaches \(\pi\) (Fig 6), so the maximum value of phase error has to be smaller than \(\pi\). Having the maximum value of phase error from (13), we have (33).

\[ \Delta \omega_{\text{slipping}} \leq \frac{I_p R_p K_{vco}}{2} \sqrt{\frac{8J_p K_{vco}}{2C_p}} \] (33)

In frequency steps greater than the (33), BBPLL will experience cycle slipping. Simulations all verify this exactly. Using (33), we can design BBPLL without cycle slipping for frequency steps.

### IV. SIMULATION RESULTS

To evaluate the proposed analysis and its closed form results, many simulations are performed for different values of input frequency step \(\Delta \omega\), current \(I_p\), resistance \(R_p\), capacitor \(C_p\), and \(K_{vco}\).

In this paper a BBPLL-based CDR with an Alexander PD and first order filter is simulated in MATLAB SIMULINK, to evaluate the analysis and modeling techniques presented. TableI gives simulation parameters used in this paper.

Note that the proposed analysis in this paper holds for different values of circuit parameter, big or small. Since BBPLL is a nonlinear system, all its transient time characteristics depend on the input step size; this can be seen from equations obtained in sections 2.1; all they are increasing function of input frequency step. Due to this, many different experiments are performed for different input frequency step sizes. All transient features like rise time, peak time, maximum value of control voltage and locking time are calculated in all experiments. Also some different experiments were performed in different input frequencies (bit rate) considering the input data signal as shown in Fig 3. The calculated locking time by the proposed equations (30) is compared with simulation results for different input frequency step sizes. These comparisons are illustrated in Fig 7 which shows the high accuracy of proposed method. Fig 7 shows that BBPLL does not experience cycle slipping for input frequency steps smaller than 13MHz in this experiment; this is exactly the same as frequency step calculated by (33). Also an input frequency step not causing cycle slipping was considered and the calculated locking times are compared with simulation results for different values of loop capacitor. These comparisons are shown in Fig 8(a). As Fig 8(a) shows, increasing loop filter capacitor, locking time increases. As the other experiment, we simulated BBPLL for different values of loop filter resistance shown in Fig 8(b). Fig 8(b) shows that increasing resistance, locking time decreases. All these results have high accuracy. The calculated maximum value of control voltage from (13) is compared to simulation results for different values of \(I_p\) and \(R_p\). These comparisons are shown in Fig 9(a) and (b). Fig 9 shows that increasing these two parameters the maximum value of control voltage decreases and larger values of these parameters cause BBPLL does not experience cycle slipping; expression (33) verifies this. The closed form equations obtained in this paper can help us to design BBPLL with specific transient characteristics. For example, we have a BBPLL based CDR with VCO gain of 200MHz/V and current source of 40mA. Assume we are to design the parameters to have the worst case locking time of 100us for maximum input frequency step of 5MHz without cycle slipping. We can simply find the values of \(C_p\) and \(R_p\) using equations mentioned in (30) and (33). Note that we adjust the number of transient intervals, \(n\). For \(n=1\) the unknowns of loop filter are simply calculated; \(R_p=610\Omega\) and \(C_p=77\mu F\). It can simply be verified with Simulation. As the other experiments we examined the BBPLL transient behavior in response to frequency steps where BBPLL does not experience cycle slipping. The experiment is performed for a frequency step of size \(\Delta \omega = 10\text{MHz}\). First, we calculated \(n\), and we obtained the control voltage of VCO and the related time intervals, using the equations of (21), (23) and (25). It is shown in (34).

\[ v_{out}(t) = \begin{cases} 
0.02 + 4 \times 10^4 t & 0 \leq t \leq 0.4us \\
0.14 - 4 \times 10^4 t & 0.4us \leq t \leq 0.6us \\
0.1 & t \geq 0.6us 
\end{cases} \] (34)

In (34), in times greater than locking time \((t \geq 0.6us)\), the control voltage is equal to the final value \(2\Delta \omega/K_{vco}\). Equation (34) has been plotted along with simulation result in Fig 10 that shows the high accuracy of equations. TableII shows the comparison between simulation and the proposed analysis results for different values of frequency step. Frequency step sizes have been chosen arbitrary between 5MHz to 13MHz. The transient time features are calculated by equations mentioned in (32), (12), (13) and (30). The results shown in the table show that the increase of input frequency step causes increase of rise time, peak time, maximum control voltage and locking time. Comparison between estimated and
Fig 7. Comparison of simulation and analysis results of locking time in response frequency steps without cycle slipping.

Fig 8. Comparison of simulation and analysis results of locking time. (a) Locking time versus capacitor. (b) Locking time versus resistance.

Table I. Simulation Parameters

<table>
<thead>
<tr>
<th>Simulation Parameters</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Resistance, $R_p$</td>
<td>500Ω</td>
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<tr>
<td>Capacitor, $C_p$</td>
<td>100pf</td>
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<tr>
<td>Current, $I_p$</td>
<td>40uA</td>
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<tr>
<td>VCO gain, $K_{VCO}$</td>
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<tr>
<td>VCO Frequency</td>
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Fig 9. Comparison of simulation and analysis results of maximum value of control voltage. (a) versus current. (b) versus resistance.

Fig 10. Comparison between the analytical result and simulation output of control voltage in response to $\Delta \omega = 10\text{MHz}$.

-locking time. Comparison between estimated and real values shows that the difference between precise and calculated results is negligibly small and proposed method has a high accuracy. Consequently we can easily find all important times and voltages in transient region by proposed method in this paper.
Table II: Comparison between simulation and calculated results when cycle slipping does not occur

<table>
<thead>
<tr>
<th>$\Delta \omega$ MHz</th>
<th>Simulation results</th>
<th>Calculated results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$t_{rise}$ ns</td>
<td>$t_p$ ns</td>
</tr>
<tr>
<td>5</td>
<td>75</td>
<td>152</td>
</tr>
<tr>
<td>8</td>
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<td>302</td>
</tr>
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<tr>
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<td>250</td>
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<tr>
<td>13</td>
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</tbody>
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V. CONCLUSION

This paper has presented a novel method to derive exact enough analytical equations for the transient response of BBPLL without cycle slipping in response to frequency step inputs. We could model the BBPLL with first order filter with high accuracy and we derived all important times and voltages along with an expression for maximum frequency step size in which cycle slipping does not occur. Nonlinear behavior of the BBPLL can be explained easily with the presented equations. This method can provide insight into BBPLL with different BPDs which can help designers for better and much easier designs.

REFERENCES